CLAIMS

What is claimed is:

1. A data triggered phase locked loop (PLL) comprises:

phase detector operably coupled to determine a phase difference between transitions of a data signal and a feedback signal;

charge pump operably coupled to convert the phase difference into a charge pump current;

loop filter operably coupled to convert the charge pump current into a control voltage;

voltage controlled oscillator operably coupled to convert the control voltage into a recovered clock, wherein feedback signal is derived from the recovered clock; and

edge detection module operably coupled to detect missing transitions of the data signal and to alter at least one of the phase difference and charge pump current based on the missing transitions such that bandwidth of the data triggered PLL remains substantially constant for varying data signal transition densities.

2. The data triggered PLL of claim 1, wherein the edge detection module functions to:

compare transitions of the recovered clock with transitions of the data signal;

when a transition occurs in the recovered clock and a substantially contemporaneously transition does not occur in the data signal, indicate a missing transition of the data signal;

increment a missing transition count of the data signal based on the indication of the missing transition until a transition of the data signal occurs substantially contemporaneously with another transition of the recovered clock to produce an accumulated missing transition count; and

at each transition of the data signal, establish a phase error scaling factor based on the accumulated missing transition count and a phase error-to-missing transition relationship.

3. The data triggered PLL of claim 2, wherein the establishing the phase error scaling factor comprises:

establishing a normalized phase error in accordance with the accumulated missing transition count as the phase error-to-missing transition relationship, wherein the normalized phase error corresponds to (n+2)/2 for [0 ... n], wherein n corresponds to a numerical value of the accumulated missing transition count; and

summing the normalized phase error to produce the phase error scaling factor.

4. The data triggered PLL of claim 2, wherein the establishing the phase error scaling factor comprises:

providing a mathematical function that relates phase error to number of missing transitions as the phase error-to-missing transition relationship; and

solving the mathematical function for the accumulated missing transition count.

5. The data triggered PLL of claim 2, wherein the phase detector comprises:

phase offset module operably coupled to provide a phase offset to at least one of phase of the data signal and phase of the feedback signal based on the phase error scaling factor to produce at least one of altered phase of the data signal and altered phase of the feedback signal; and

up/down signal generation module operably coupled to produce:

an up signal when:

the altered phase of the data signal leads the phase of the feedback signal;

the phase of the data signal leads the altered phase of the feedback signal; or

the altered phase of the data signal leads the altered phase of the feedback signal; and

a down signal when:

the altered phase of the feedback signal leads the phase of the data signal;

the phase of the feedback signal leads the altered phase of the data signal; or

the altered phase of the feedback signal leads the altered phase of the data signal.

6. The data triggered PLL of claim 1, wherein the charge pump comprises:

a variable current source operably coupled to provide a variable source current to the loop filter based on a first state of the phase difference that corresponds to when phase of the data signal leads phase of the feedback signal, wherein magnitude of the variable source current is based on the phase error scaling factor; and

a variable current sink operably coupled to draw a variable sink current from the loop filter based on a second state of the phase difference that corresponds to when the phase of the feedback signal leads the phase of the data signal, wherein magnitude of the variable sink current is based on the missing transitions.

7. The data triggered PLL of claim 1, wherein the charge pump comprises:

a variable current source operably coupled to provide a source current during a variable source current on time to the loop filter based on a first state of the phase difference that corresponds to when phase of the data signal leads phase of the feedback signal, wherein duration of the variable source current on time during which the variable

current source provides the source current is based on the phase error scaling factor; and

a variable current sink operably coupled to draw a sink current during a variable sink current on time from the loop filter based on a second state of the phase difference that corresponds to when the phase of the feedback signal leads the phase of the data signal, wherein duration of the variable sink current on time during which the variable current sink draws the sink current is based on the missing transitions.

8. A method for recovering a clock from a data signal, the method comprises:

determining a phase error between a feedback signal and the data signal;

determining missing transitions of the data signal;

scaling the phase error based on the missing transitions to produce a scaled phase error; and

generating a recovered clock based on the scaled phase error, wherein the feedback signal is derived from the recovered clock.

9. The method of claim 8, wherein the determining the missing transitions comprises:

comparing transitions of the recovered clock with transitions of the data signal;

when a transition occurs in the recovered clock and a substantially contemporaneous transition does not occur in the data signal, indicate a missing transition of the data signal;

increment a missing transition count of the data signal based on the indication of the missing transition until a transition of the data signal occurs substantially contemporaneously with another transition of the recovered clock to produce an accumulated missing transition count.

10. The method of claim 9, wherein the scaling the phase error comprises:

establishing a normalized phase error in accordance with the accumulated missing transition count, wherein the normalized phase error corresponds to (n+2)/2 for [0 ... n], wherein n corresponds to a numerical value of the accumulated missing transition count; and

summing the normalized phase error to produce the scaled phase error.

11. The method of claim 9, wherein the scaling the phase errr comprises:

providing a mathematical function that relates phase error to number of missing transitions; and

solving the mathematical function for the accumulated missing transition count.

12. An apparatus for recovering a clock from a data signal, the apparatus comprises:

processing module; and

memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to:

determine a phase error between a feedback signal and the data signal;

determine missing transitions of the data signal;

scale the phase error based on the missing transitions to produce a scaled phase error; and

generate a recovered clock based on the scaled phase error, wherein the feedback signal is derived from the recovered clock.

13. The apparatus of claim 12, wherein the memory further comprises operational instructions that cause the processing module to determine the missing transitions by:

comparing transitions of the recovered clock with transitions of the data signal;

when a transition occurs in the recovered clock and a substantially contemporaneous transition does not occur in the data signal, indicate a missing transition of the data signal; and

increment a missing transition count of the data signal based on the indication of the missing transition until a transition of the data signal occurs substantially contemporaneously with another transition of the recovered clock to produce an accumulated missing transition count.

14. The apparatus of claim 13, wherein the memory further comprises operational instructions that cause the processing module to scale the phase error by:

establishing a normalized phase error in accordance with the accumulated missing transition count, wherein the normalized phase error corresponds to (n+2)/2 for [0 ... n], wherein n corresponds to a numerical value of the accumulated missing transition count; and

summing the normalized phase error to produce the scaled phase error.

15. The apparatus of claim 13, wherein the memory further comprises operational instructions that cause the processing module to scale the phase error by:

providing a mathematical function that relates phase error to number of missing transitions; and

solving the mathematical function for the accumulated missing transition count.